WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising:

a plurality of first capacitors that are charged during a first period;

a plurality of second capacitors provided alternately with the first capacitors, the second capacitors being charged during a second period that partially overlaps with the first period;

a first transfer device for transferring charges stored in each first capacitor to the succeeding second capacitor during a third period that is delayed from the second period by a predetermined time; and

a second transfer device for transferring charges stored in each second capacitor to the succeeding first capacitor during a fourth period that is delayed from the first period by the predetermined time.

2. The semiconductor integrated circuit according to claim 1, wherein the first transfer device includes a first NMOS transistor, a source thereof being connected to each first capacitor, a drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a third capacitor connected to a gate of the first NMOS transistor; and

a second NMOS transistor, a source thereof being connected to the source of the first NMOS transistor, a drain thereof being connected to the gate of the first NMOS transistor and a gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second period overlap each other to charge the third capacitor, and charges stored in the third capacitor are supplied to the gate of the first NMOS transistor as the first transfer device during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

3. The semiconductor integrated circuit according to claim 1, wherein the second transfer device includes a first NMOS transistor, a source thereof being connected to each second capacitor, a drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a third capacitor connected to a gate of the first NMOS transistor; and

a second NMOS transistor, a source thereof being connected to the source of the first NMOS transistor, a drain thereof being connected to the gate of the first NMOS transistor and a gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second period overlap each other to charge the third capacitor, and charges stored in the third capacitor is supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

4. The semiconductor integrated circuit according to claim 1, wherein the third period terminates by the predetermined time before the succeeding second period starts.

5. The semiconductor integrated circuit according to claim 1, wherein the fourth period terminates by the predetermined time before the succeeding first period starts.